

AMENDMENT TO THE CLAIMS

This Listing of Claims will replace all prior versions, listing, of claims in the specification.

LISTING OF CLAIMS:

Claim 1 (original) A common spacer dual gate memory cell comprising:

two bit lines on a semiconductor substrate;

a first channel for a first transistor and a second channel for a second transistor arranged in series between said two bit lines;

a first gate dielectric and a second gate dielectric above said first and second channels, respectively;

a first control gate and a second control gate above said first and second gate dielectrics, respectively; and

a spacer between said first and second control gates;

wherein at least one of said first and second gate dielectrics includes a silicon nitride.

Claim 2 (original) A memory cell according to claim 1, further comprising a punch through region between said two bit lines.

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Claim 3 (original) A memory cell according to claim 1, wherein said first control gate extends along a first direction and said second control gate extends along a second direction perpendicular to said first direction.

Claim 4 (original) A memory cell according to claim 1, wherein said second control gate has a portion crossing over above and isolated from said first control gate.

Claim 5 (original) A memory cell according to claim 1, wherein said spacer is formed on a sidewall of said first control gate.

Claim 6 (original) A memory cell according to claim 1, wherein said spacer and first control gate extend along a same direction.

Claim 7 (original) A memory cell according to claim 1, wherein said second control gate has a portion crossing over above said spacer.

Claim 8 (original) A memory cell according to claim 1, wherein said second control gate has a portion in a trench to contact said second gate dielectric.

Claim 9 (original) A memory cell according to claim 1, wherein said first and second gate dielectrics each comprises a silicon nitride.

Claim 10 (original) A memory cell according to claim 9, wherein one of said two transistors is completely turned on during the other one is read.

Claim 11 (original) A memory cell according to claim 9, wherein one of said two transistors is completely turned on during the other one is programmed.

Claim 12 (original) A memory cell according to claim 1, wherein one of said first and second gate dielectrics includes an oxide only.

Claim 13 (original) A memory cell according to claim 12, wherein said oxide gated transistor is turned on during the other one is programmed.

Claim 14 (original) A memory cell according to claim 12, wherein said oxide gated transistor is turned on during the other one is read.

Claim 15 (original) A memory cell according to claim 1, wherein silicon nitride gated transistor is programmed with two charge storage locations.

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Claim 16 (original) A memory cell according to claim 15, wherein said two charge storage locations are programmed with a threshold voltage substantially different from each other.

Claim 17 (original) A memory cell according to claim 1, wherein silicon nitride gated transistor is programmed with one charge storage location next to said spacer.

Claims 18-23 (canceled).